REMARKS

By this Amendment, Applicants amend claims 10 and 14, cancel claim 12 without prejudice of the subject matter recited therein, and add new claims 23 and 24. Claims 1-10, 14, 15, and 17-24 are pending with claims 1-9 and 20 being withdrawn.

In the Office Action, the Examiner objected to claim 10 because of informalities; rejected claims 10, 14, 15, 19, 21, and 22 under 35 U.S.C §103(a) as unpatentable over Amos et al., U.S. Patent No. 6,846,734, ("*Amos*") in view of Lochtefeld et al., U.S. Patent Publication No. 2006/0024869, ("*Lochtefeld*"); rejected claim 12 under 35 U.S.C §103(a) as unpatentable over *Amos* in view of *Lochtefeld* and further in view of Thakur, U.S. Patent No. 6,028,002, ("*Thakur*"); and rejected claim 18 under 35 U.S.C §103(a) as unpatentable over *Amos* in view of *Lochtefeld* and further in view of remarks.

In response, Applicants submit that the rejections under sections 103(a) are improper and that claims 10, 14, 15, 17-19, and 21-24 are allowable over the cited documents. More particularly, Applicants submit that the rejections under section 103(a) are improper because the cited documents fail to teach or suggest all the elements of 10, 14, 15, 17-19, and 21-24. M.P.E.P § 2143, ed. 8, r. 5, p. 2100-126 (August 2006).

Claim 10 is directed to a method for manufacturing a semiconductor device comprising, *inter alia*, "**forming a layer of silicided gate electrode material over said gate oxide**, comprising: forming a layer of polysilicon material over said layer of gate oxide material, forming a layer of an alloy comprising a first metal and a second metal over said layer of polysilicon material, and **annealing said layer of said alloy**

comprising said first metal and said second metal to from a layer of silicided gate electrode material including said first metal and said second metal; and patterning said layer of silicided gate electrode material to form said silicided gate electrode" (emphasis added). In other words, claim 10 recites, among other things, forming a layer of silicided gate electrode material using an alloy of a first and second metal prior to patterning the layer of silicided gate electrode material to form the gate electrode.

By forming the silicided gate electrode material prior to forming the gate, the method recited in claim 10 reduces the line width effect problems experienced in semiconductor manufacturing. Additionally, because of this process order, the method recited in claim 10 reduces silicidation problems due to concurrently formed silicided source/drain contact regions for the source/drain regions. Particularly, the silicided source/drain contact regions may not be required to be formed simultaneous with the layer of silicided gate electrode material. As such, the formation of one does not affect the formation of the other.

In contrast, the cited documents fail to teach or suggest these recitations of claim 10. Particularly, *Amos* discloses forming a silicided gate electrode using an alloy. *Amos*, col. 8-9. *Amos*, however, discloses that the initial FET structure, including the gate structure, is formed first. *Amos*, col. 8, ll. 34-49. Then, the gate is silicided after the gate structure has already been formed. *Amos*, col. 9, ll. 10-30. Accordingly, *Amos* fails to teach or suggest all the elements of claim 10.

Furthermore, the other cited documents fail to teach or suggest these claims elements. Particularly, *Lochtefeld* fails to disclose siliciding a gate material using an

alloy prior to forming the gate structure. *Lochtefeld*, ¶56. Likewise, *Thakur* fails to disclose siliciding a gate material using an alloy prior to forming the gate structure. *Thakur*, col. 2, ll. 32-56.

Therefore, the cited documents fail to teach or suggest all the elements of claim 10. Accordingly, the rejections under section 103(a) are improper and should be withdrawn. As such, Applicants submit that claim 10 is allowable over the cited documents. Claims 14, 15, 17-19, and 21-24 are allowable at least due to their dependence from allowable claim 10.

In view of the foregoing, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

If the Examiner believes that additional discussions or information might advance the prosecution of the instant application, the Examiner is invited to contact the undersigned at the telephone number listed below to expedite resolution of any outstanding issues.

Please grant any extensions of time required to enter this response and charge any additional required fees to deposit account 20-0668 (in the name of Texas Instruments) or, if necessary, to our deposit account 50-2961.

Respectfully submitted,

Dated: January 22, 2007

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